LISTING OF THE CLAIMS

1. (original) A method for reducing diagnostic time of a photon detecting integrated circuit tester, the method comprising:

processing a CAD database associated with an integrated circuit; and

defining at least one CAD layer from the CAD database, the at least one CAD layer identifying at least one expected photon emission source of the integrated circuit.

2. (original) The method of claim 1 further comprising:

aligning the tester with the at least one CAD layer to correlate the tester with the at least one expected photon emission source.

3. (original) The method of claim 2 further comprising:

identifying photon emissions from the at least one expected photon emission source, the photon emissions detected by the tester during operation of the integrated circuit.

4. (original) The method of claim 3 wherein the operation of identifying photon emissions from the at least one expected photon emission source comprises receiving photon emission through the a semiconductor substrate of the integrated circuit.

5. (original) The method of claim 3 wherein the photon emissions detected by the tester during operation of the integrated circuit in a test loop.

6. (original) The method of claim 3 further comprising:

determining at least one operating characteristic of the at least one expected photon emission source.

7. (original) The method of claim 6 wherein the operation of determining the at least one operating characteristic comprises determining timing measurements employing a single photon counting technique.

8. (original) The method of claim 7 further comprising:

comparing the at least one operating characteristic of the at least one expected photon emission source with a simulation of the operating integrated circuit.

9. (original) The method of claim 8 wherein the simulation is in an optical waveform format.

10. (original) The method of claim 8 wherein the simulation is in a voltage level format.

11. (original) The method of claim 6 wherein the at least one expected emission source is at least one transistor.

12. (original) The method of claim 11 wherein the operation of comparing the operating characteristics of the least one transistor includes identifying transistors that are and are not working in accordance with the simulation.

13. (original) The method of claim 11 wherein the operation of comparing the operating characteristics of the least one transistor includes identifying emission peaks of transistors that are or are not present in the simulation.

14. (original) The method of claim 11 wherein the operation of comparing the operating characteristics of the least one transistor includes identifying differences between operating characteristics of the at least one expected photon emission source and the simulation.

15. (original) The method of claim 11 wherein the operation of determining the at least one operating characteristic of the at least one expected photon emission source comprises determining a commutation timing of the at least one transistor.

16. (original) The method of claim 1 wherein the at least one expected emission source is a MOS device.

17. (original) The method of claim 1 wherein the at least one expected emission source is a PMOS device.

18. (original) The method of claim 1 wherein the at least one expected emission source is a NMOS device.

19. (original) The method of claim 1 wherein the at least one expected emission source is a nFET.

20. (original) The method of claim 1 wherein the at least one expected emission source is a pFET.

21. (original) The method of claim 1 wherein the tester comprises an optical detector.

22. (original) The method of claim 1 wherein the tester comprises a laser scanning microscope.

23. (original) The method of claim 1 wherein the tester comprises a picosecond imaging circuit analysis detector.

24. (original) The method of claim 1 wherein the tester comprises a static emission detector.

25. (original) The method of claim 1 wherein the tester comprises a superconducting single photon detector.

26. (original) A method of processing an integrated circuit CAD database for use in testing the integrated circuit with an imaging optical detector comprising:

identifying the location of at least one transistor in the integrated circuit CAD database; and

defining at least one photon detection location as a function of the location of the at least one transistor.

27. (original) The method of claim 26 wherein the operation of identifying the locations of the at least one transistor in the integrated circuit CAD database comprises identifying a location of a gate associated with the at least one transistor.

28. (original) The method of claim 27 wherein the operation of identifying the locations of transistors in the integrated circuit CAD database comprises identifying the location of a source associated with the at least one transistor.

29. (original) The method of claim 28 wherein the operation of identifying the locations of transistors in the integrated circuit CAD database comprises identifying the location of a drain associated with the at least one transistor.

30. (original) The method of claim 29 wherein the operation of defining at least one photon detection location as a function of the locations of the at least one transistor comprises defining at least one photon detection location as a function of the location the gate, the drain, and the source or the at least one transistor.

31. (original) The method of claim 30 wherein the at least one transistor is a PMOS transistor.

32. (original) The method of claim 31 wherein the at least one transistor is a NMOS transistor.

33. (original) The method of claim 32 further comprising:

identifying whether the at least one photon detection location is associated with the PMOS or the NMOS transistor.

34. (original) The method of claim 33 wherein the operation of identifying the location of the at least one transistor in the integrated circuit CAD database is performed using at least one Boolean operation.

35. (original) The method of claim 33 wherein the integrated circuit CAD database information comprises an identification of a NMOS gate, a NMOS drain, and a NMOS source.

36. (original) The method of claim 35 wherein the NMOS gate information includes a polysilicon polygon layer and a P substrate polygon layer, the NMOS drain information includes an N diffusion polygon layer and a P substrate polygon layer, and the NMOS source layer includes an N diffusion polygon layer and a P substrate polygon layer.

37. (original) The method of claim 36 wherein the operation of identifying the location of the at least one transistor in the integrated circuit CAD database is performed using at least one Boolean operation further includes the operation of applying at least one Boolean operation to the NMOS gate information.

38. (original) The method of claim 37 wherein the at least one Boolean operation comprises:

NMOS gate = Polysilicon polygon layer AND Psubstrate polygon layer; and

NMOS Drain and Source = Ndiffusion polygon layer AND Psubstrate polygon layer.

39. (original) The method of claim 38 further comprising:

generating a CAD file with NMOS layer information as a function of the at least one Boolean operation.

40. (original) The method of claim 32 wherein the integrated circuit CAD database information further comprises an identification of a PMOS gate, a PMOS drain, and a PMOS source.

41. (original) The method of claim 40 wherein the PMOS gate information includes a polysilicon polygon layer and an Nwell polygon layer, the PMOS drain information includes a Pdiffusion polygon layer and a Nwell polygon layer, and the NMOS source layer includes an Pdiffusion polygon layer and a Nwell polygon layer.

42. (original) The method of claim 41 wherein the operation of identifying the location of the at least one transistor in the integrated circuit CAD database is performed using at least one Boolean operation further includes the operation of applying the at least one Boolean operation to the PMOS gate information.

43. (original) The method of claim 42 wherein the at least one Boolean operation comprises:

PMOS gate = Polysilicon polygon layer AND Nwell polygon layer; and

PMOS Drain and Source = Pdiffusion polygon layer AND Nwell polygon layer.

44. (original) The method of claim 43 further comprising:

generating a CAD file with NMOS layer information as a function of the at least one Boolean operation.

45. (original) The method of claim 26 wherein the at least one photon detection location comprises a generally rectangular photon emission detection window.

46. (original) The method of claim 45 wherein the generally rectangular window defines an area associated with at least a portion of a gate region of a MOS transistor.

47. (original) The method of claim 46 wherein the generally rectangular window further defines an area associated with at least a portion of the gate region of a MOS transistor and an adjacent pinch-off region.

48. (original) The method of claim 47 further comprising scaling the generally rectangular window.

49. (original) The method of claim 48 wherein the generally rectangular window is scaled in the range of between about 2 microns and about 3 microns.

50. (original) The method of claim 49 wherein the generally rectangular window is symmetrically scaled.

51. (original) The method of claim 50 wherein the generally rectangular window is scaled-up as a function of a thickness of the substrate of the integrated circuit.

52. (original) The method of claim 51 wherein the generally rectangular window is scaled-up or scaled-down as a function of a separation distance of the at least one transistor.

53. (original) The method of claim 26 further comprising:

characterizing the operation of an integrated circuit as a function of the at least one photon detection location.

54. (original) The method of claim 53 further comprising:

testing the integrated circuit with an optical detector comprising:

obtaining an image of the integrated circuit;

aligning the image with the CAD database information for the integrated circuit;

aligning the at least one photon detection location with the location of the at least one transistor; and

detecting photon emission in the at least one photon detection location during operation of the integrated circuit.

55. (original) The method of claim 54 further comprising:

examining photon emissions in the at least one photon detection location.

56. (original) The method of claim 55 further comprising:

obtaining photon emissions during operation of the integrated circuit in a test loop.

57. (original) The method of claim 54 wherein the optical detector comprises an imaging optical detector.

58. (original) The method of claim 57 wherein the imaging optical detector comprises a picosecond imaging circuit analysis detector.

59. (original) The method of claim 56 further comprising:

comparing the photon emissions detected in the at least one photon detection location during operation of the integrated circuit with at least one expected result.

60. (original) The method of claim 59 wherein the operation of comparing the photon emissions detected in the at least one photon detection location during operation of the integrated circuit with at least one expected result further comprises determining faults and defects of the integrated circuit.

61. (original) The method of claim 59 wherein the operation of comparing the photon emissions detected in the at least one photon detection location during operation of the integrated circuit with at least one expected result further comprises debugging the design of the integrated circuit.

62. (original) The method of claim 59 wherein the operation of comparing the photon emissions detected in the at least one photon detection location during operation of the integrated circuit with at least one expected result further comprises separating design errors and process defects.

63. (original) The method of claim 59 wherein the operation of comparing the photon emissions detected in the at least one photon detection location during operation of the integrated circuit with at least one expected result further comprises identifying an inaccurate model of the integrated circuit.